

FIG. 1
(Prior Art)

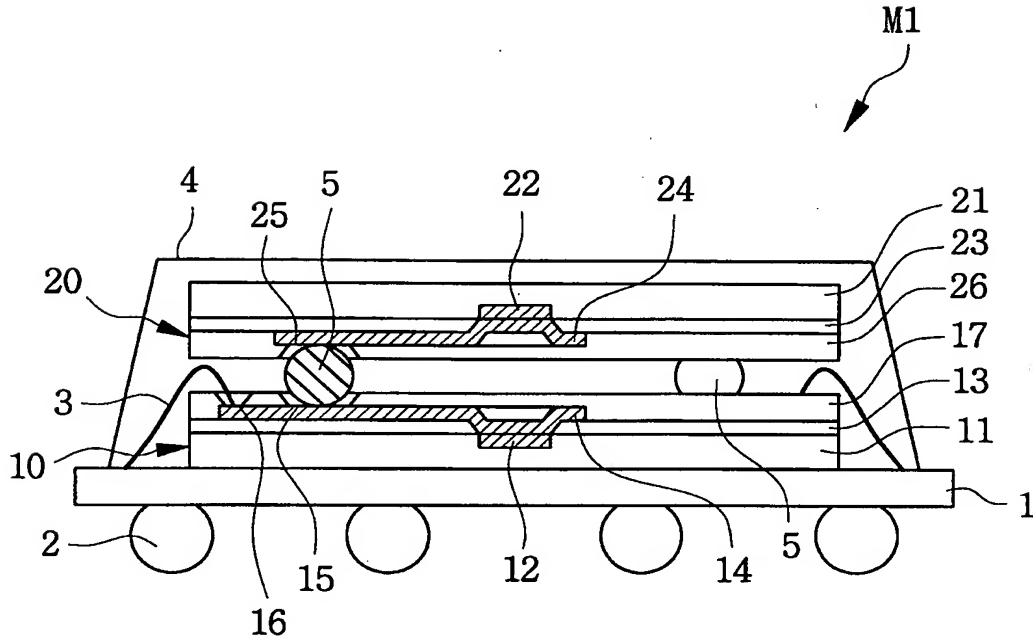


FIG. 2

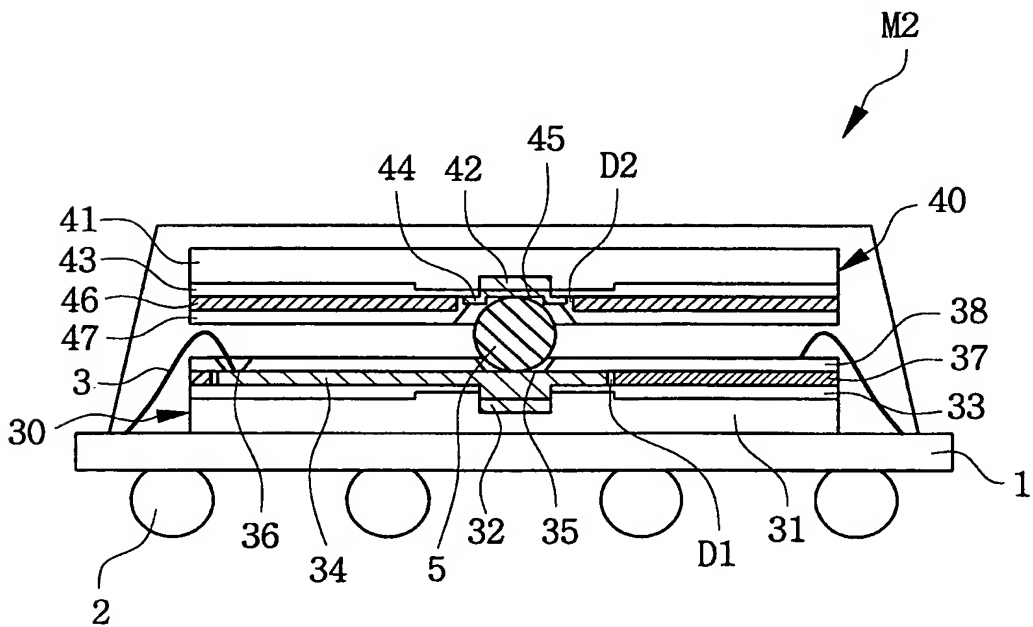
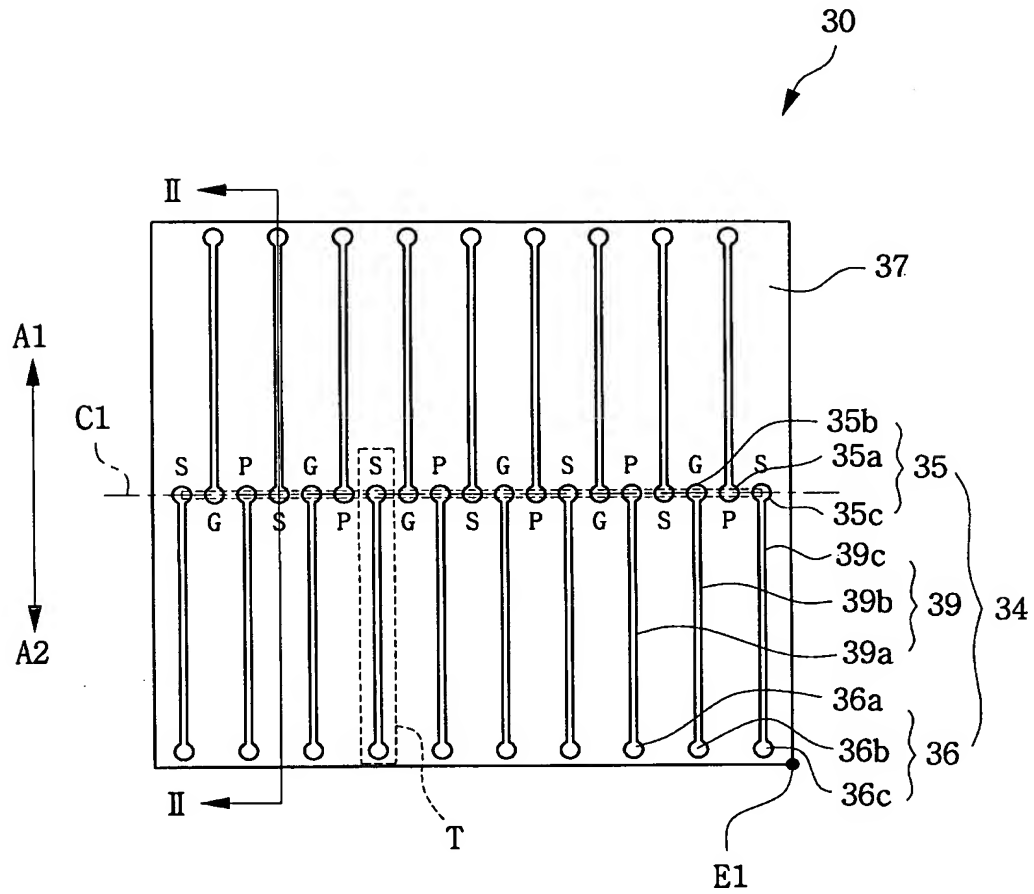


FIG. 3A



40

II

46

C2

S G P S G P S G P S G P S G P S G P S

45c

45b

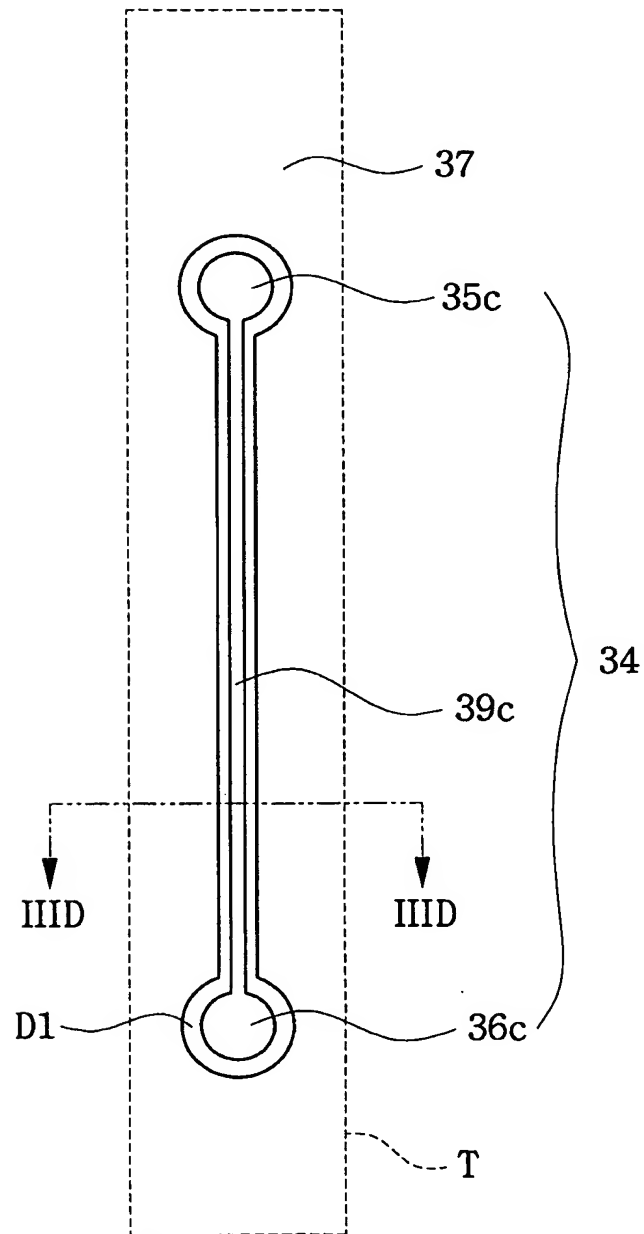
45a

F1

II

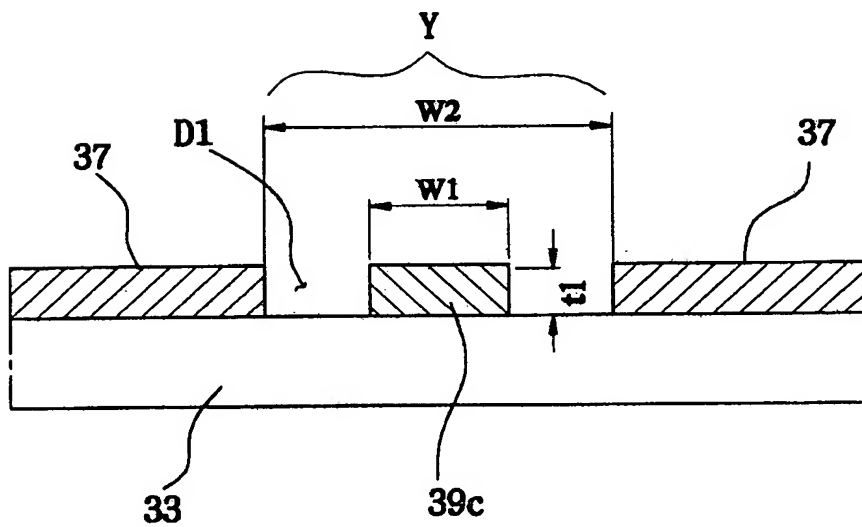
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FIG. 3C



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FIG. 3D



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FIG. 4

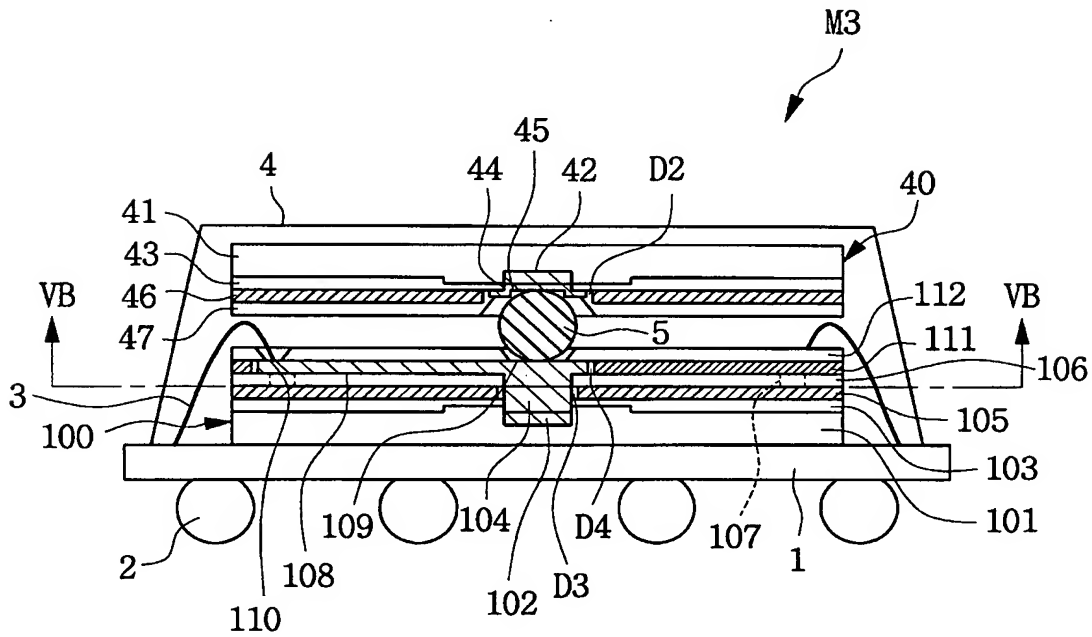


FIG. 6

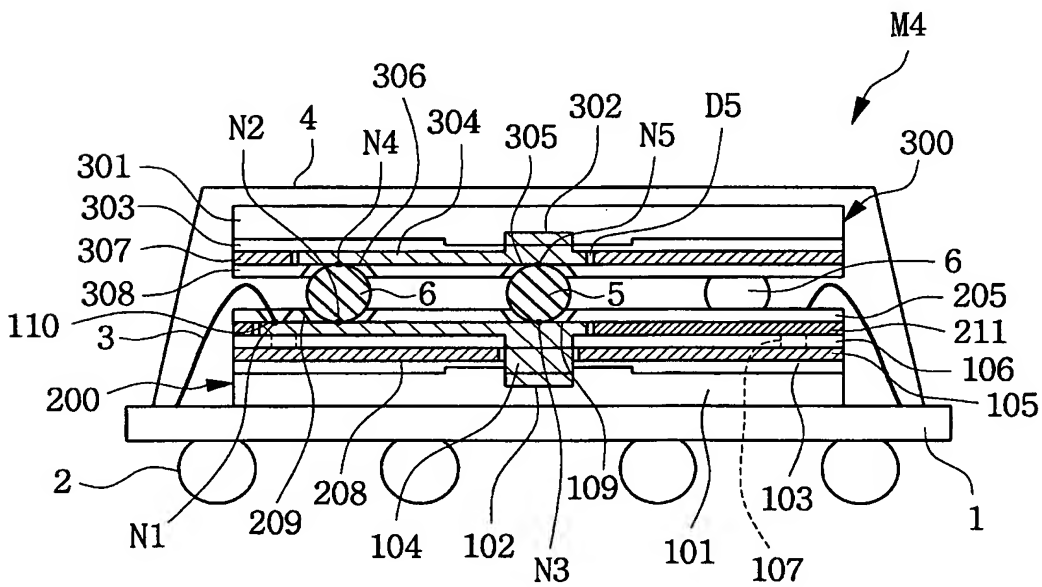


Diagram illustrating a plan view of a semiconductor device 100. The device features a grid of elements labeled G, P, and S. The grid is organized into rows and columns. The top row contains elements G, S, P, G, S, P, G, S, P. The bottom row contains elements S, P, G, S, P, G, S, P, G. The central horizontal strip 109 contains elements S, G, P, G, P, S, G, P, G, P, S, G, P, G, P, S. The vertical strips 108 contain elements S, P, G, S, P, G, S, P, G. The bottom row 110 contains elements S, P, G, S, P, G, S, P, G. The device is divided into regions by dashed lines A3, A4, and C3. Arrows IV indicate horizontal directions. A specific element is labeled E2.

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FIG. 5B

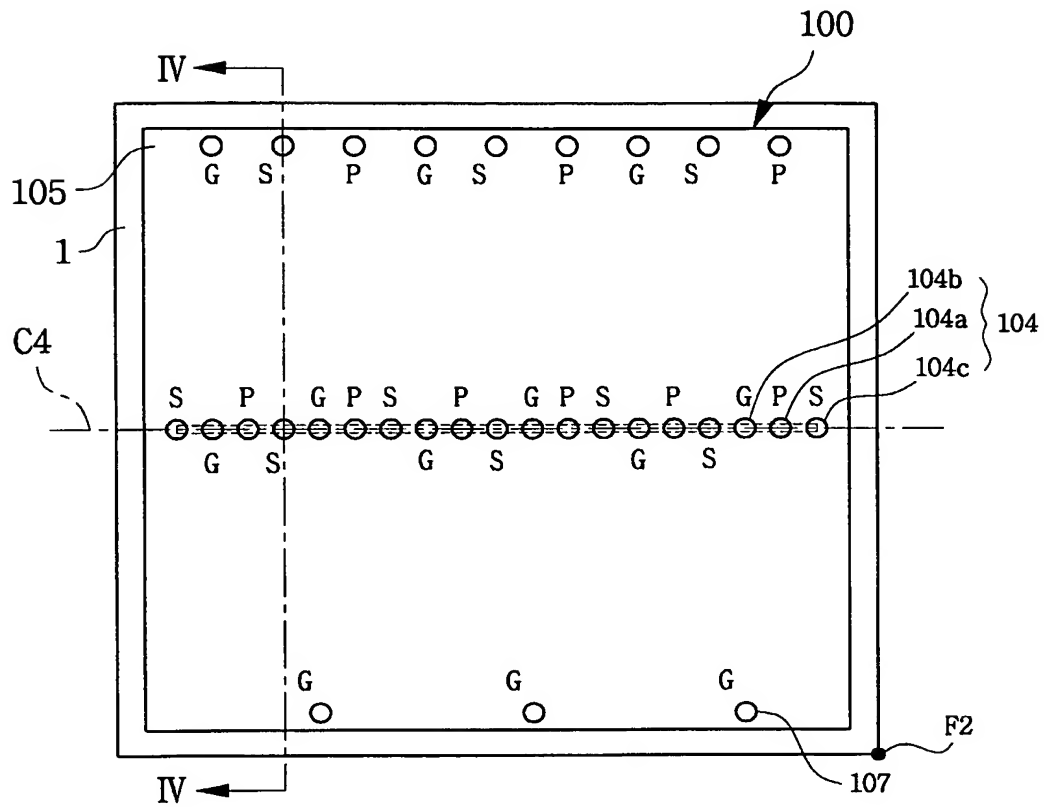


Diagram illustrating a plan view of a semiconductor device 200. The device features a central horizontal region 109, vertical regions 110, and a top region 211. The central region 109 contains a series of gates (G) and source/drain regions (S) separated by passivation (P). The vertical regions 110 also contain gates (G) and source/drain regions (S) separated by passivation (P). The top region 211 contains gates (G) and source/drain regions (S) separated by passivation (P). Arrows A5 and A6 indicate directions. Labels E3, C5, and VI are also present.

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FIG. 8A

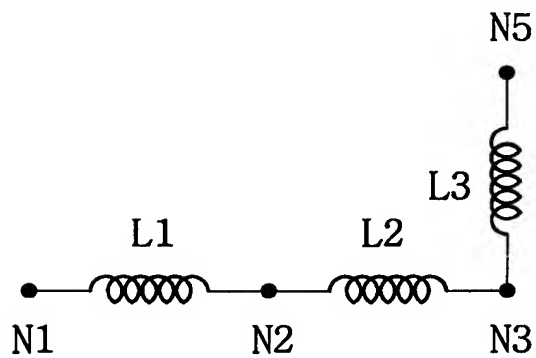
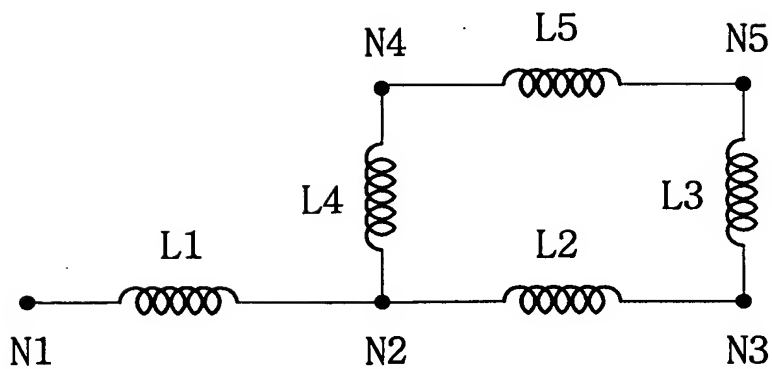


FIG. 8B



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FIG. 9A

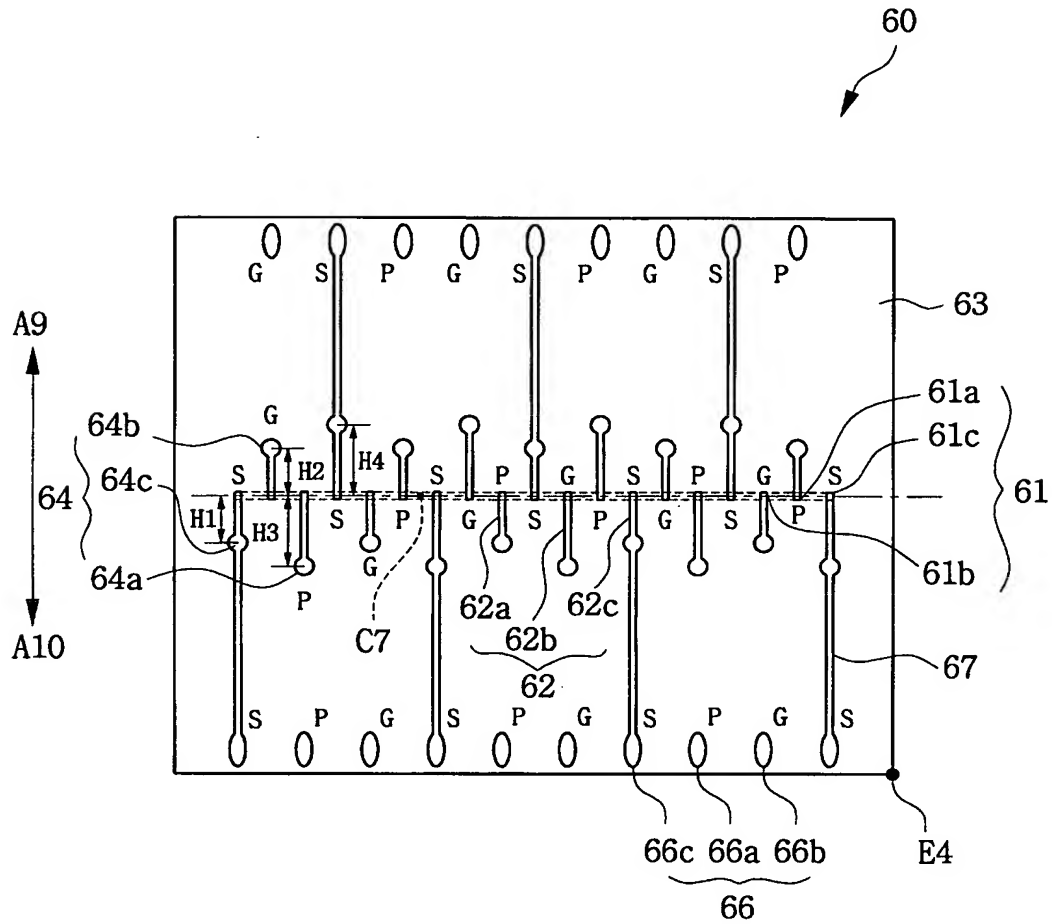
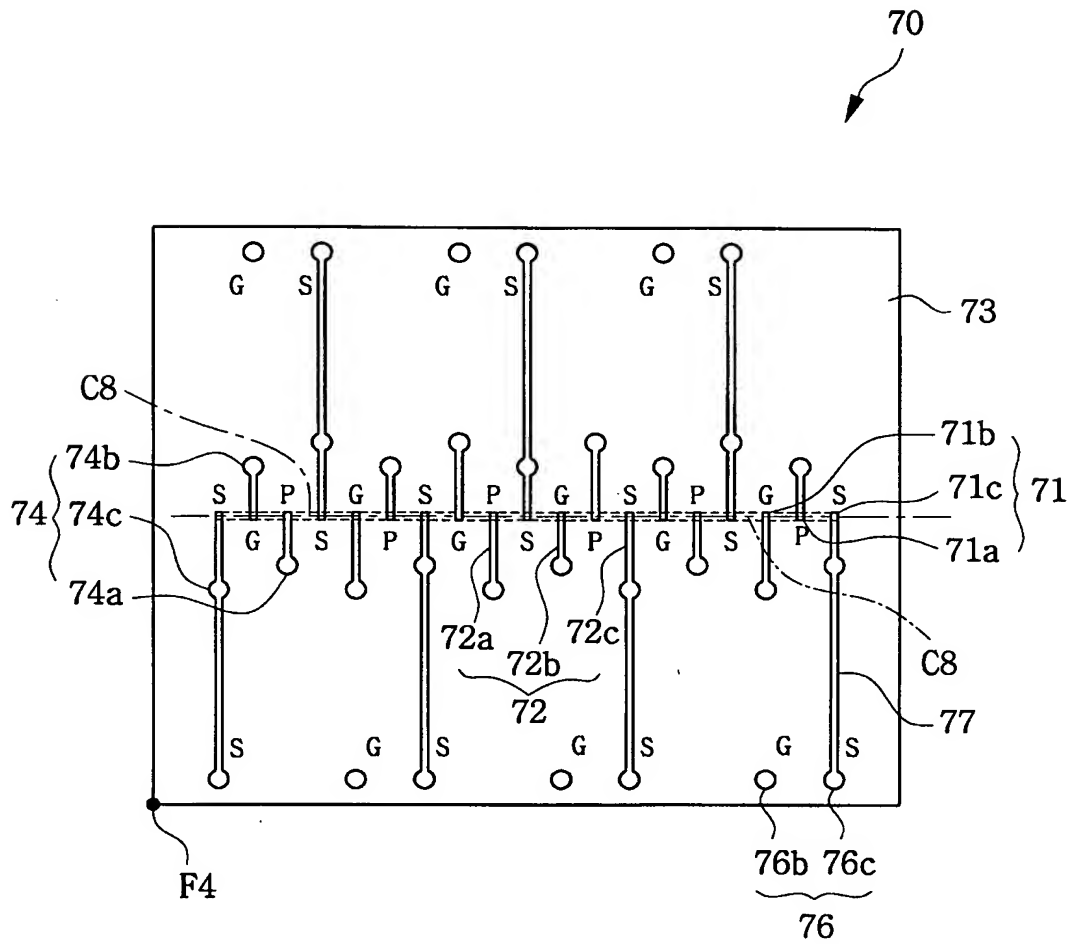


FIG. 9B



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FIG. 10A

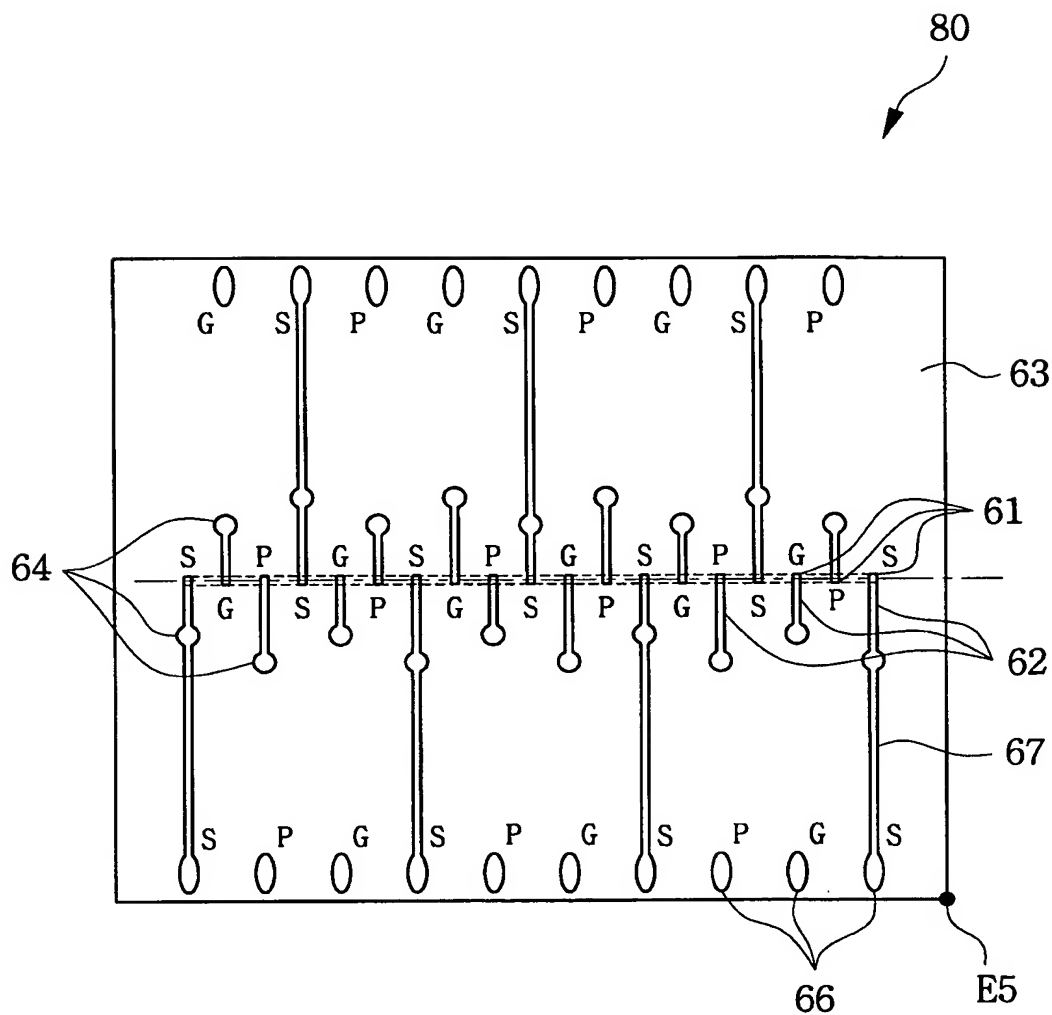
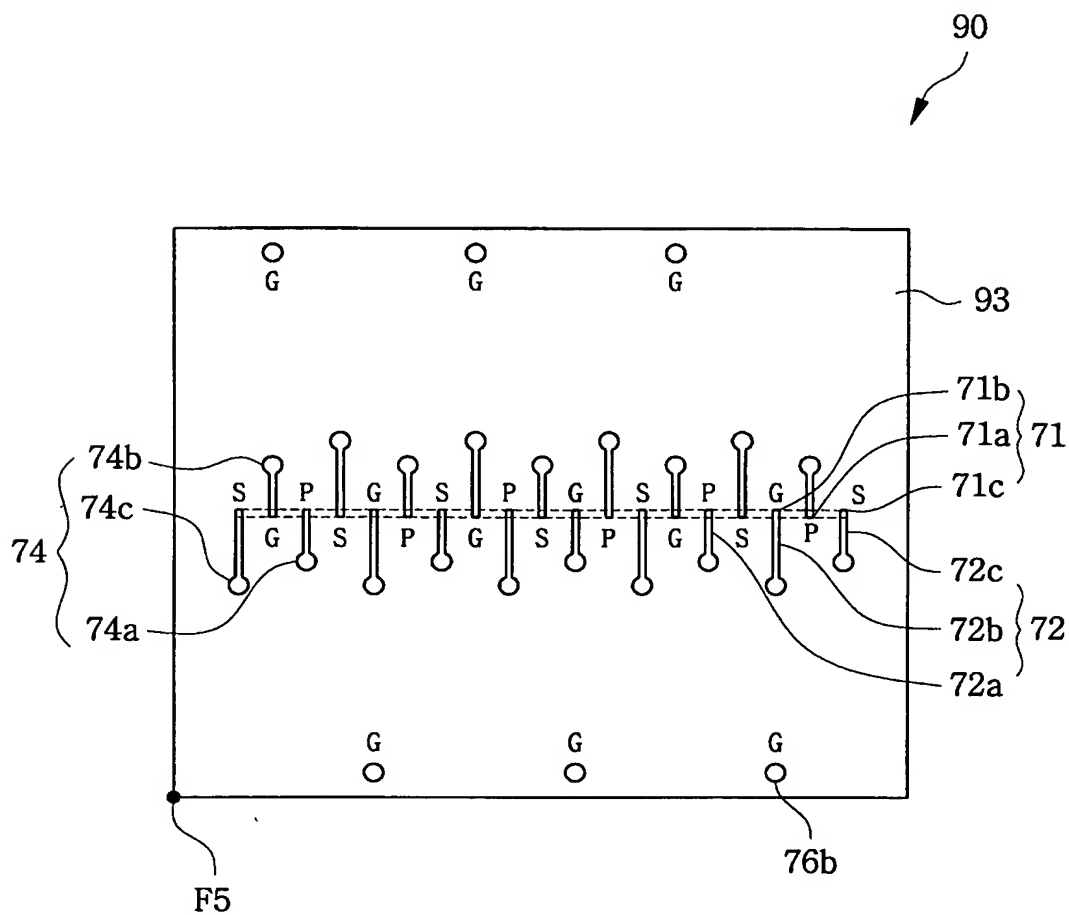


FIG. 10B



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FIG. 11A

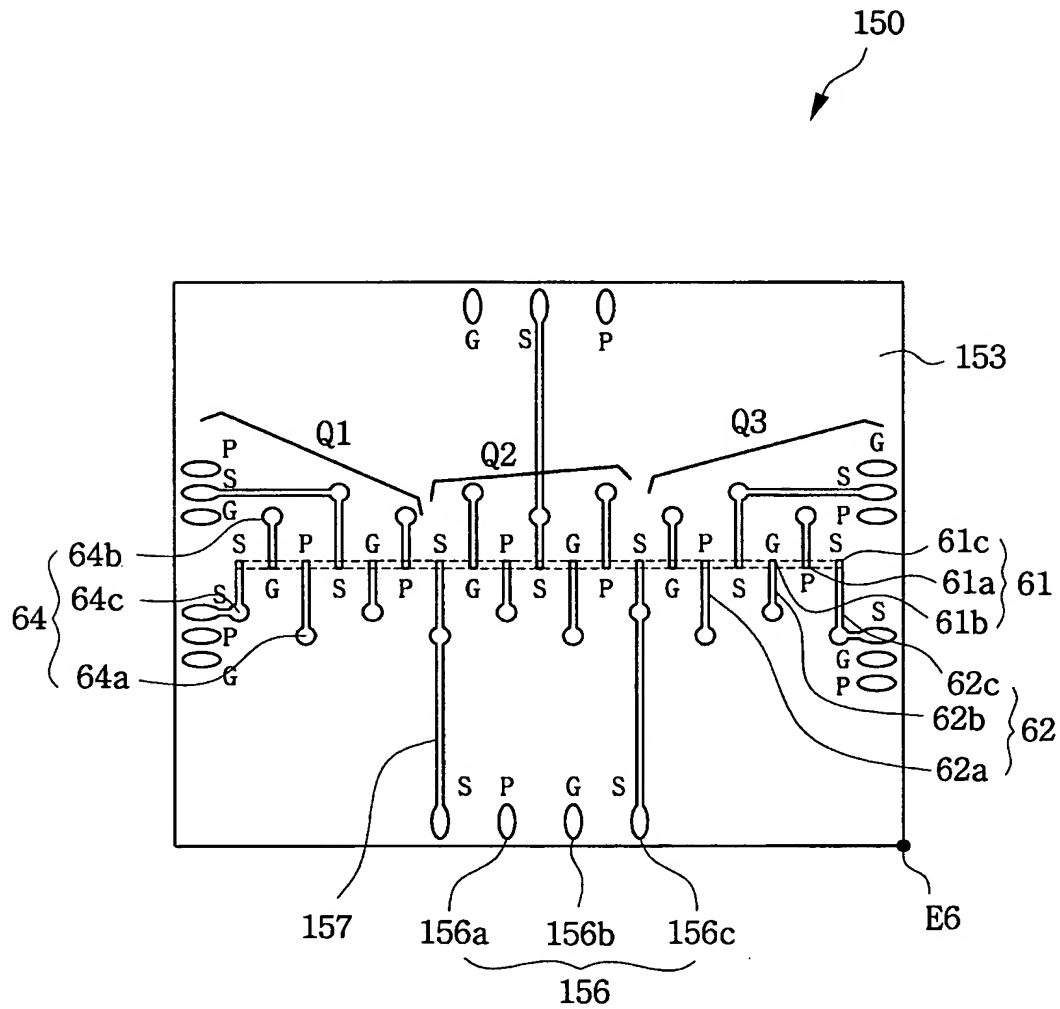
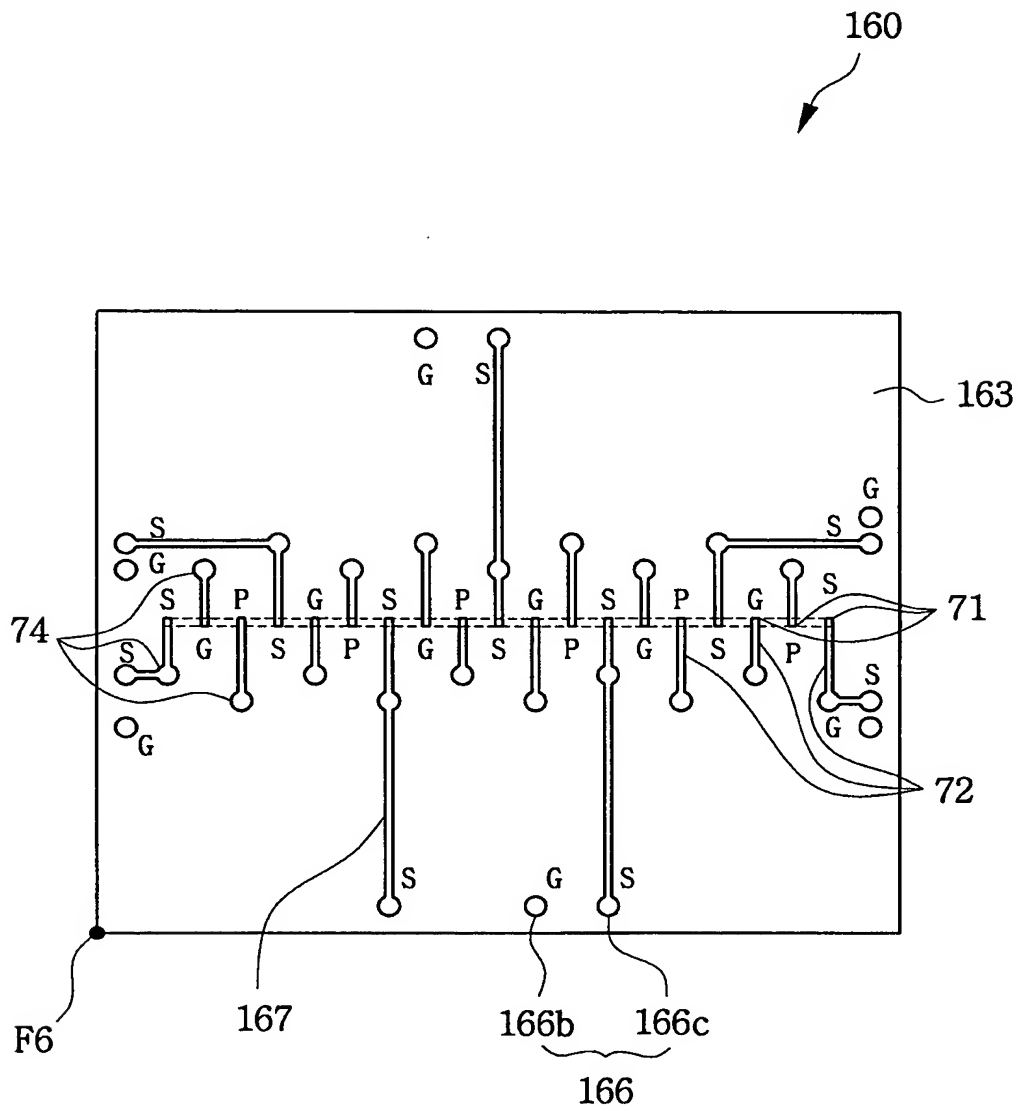


FIG. 11B



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FIG. 12A

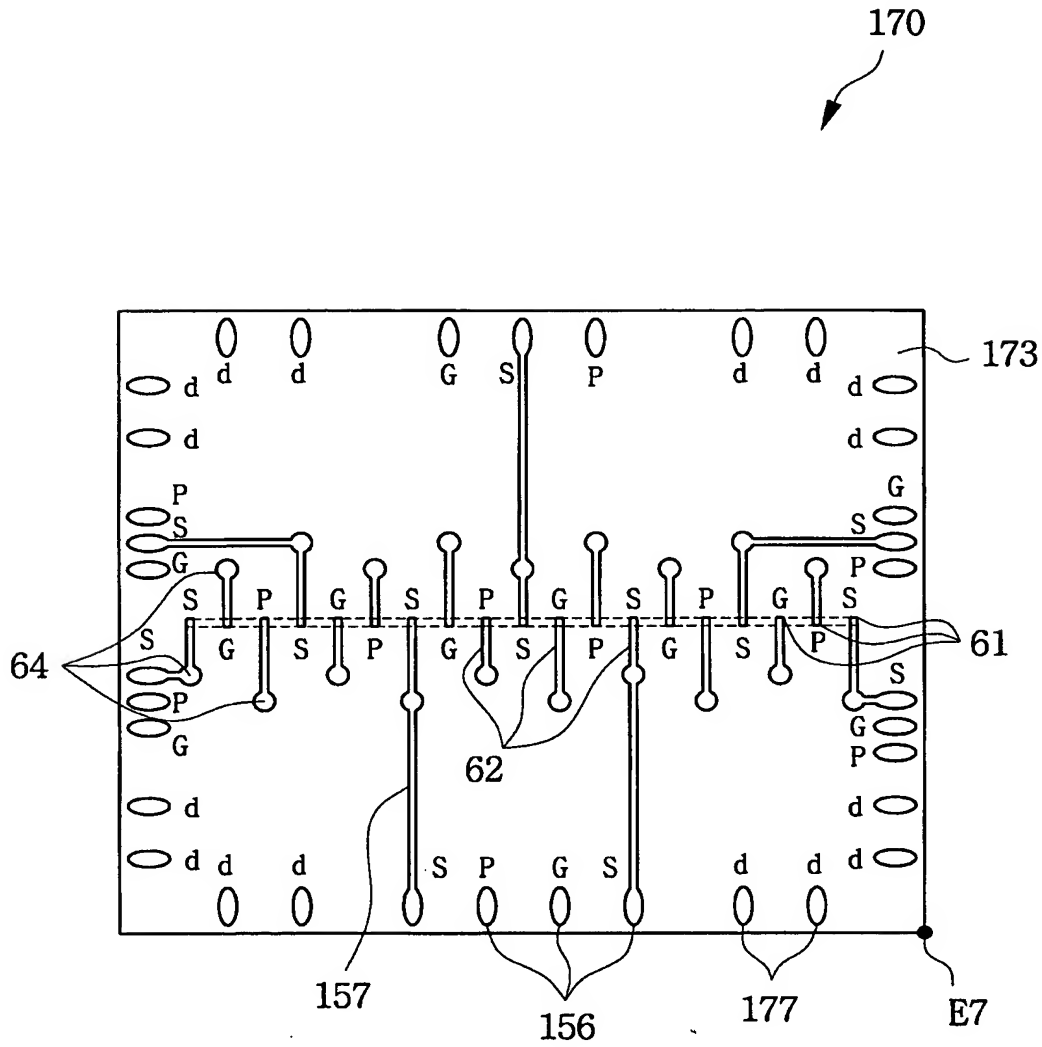


FIG. 12B

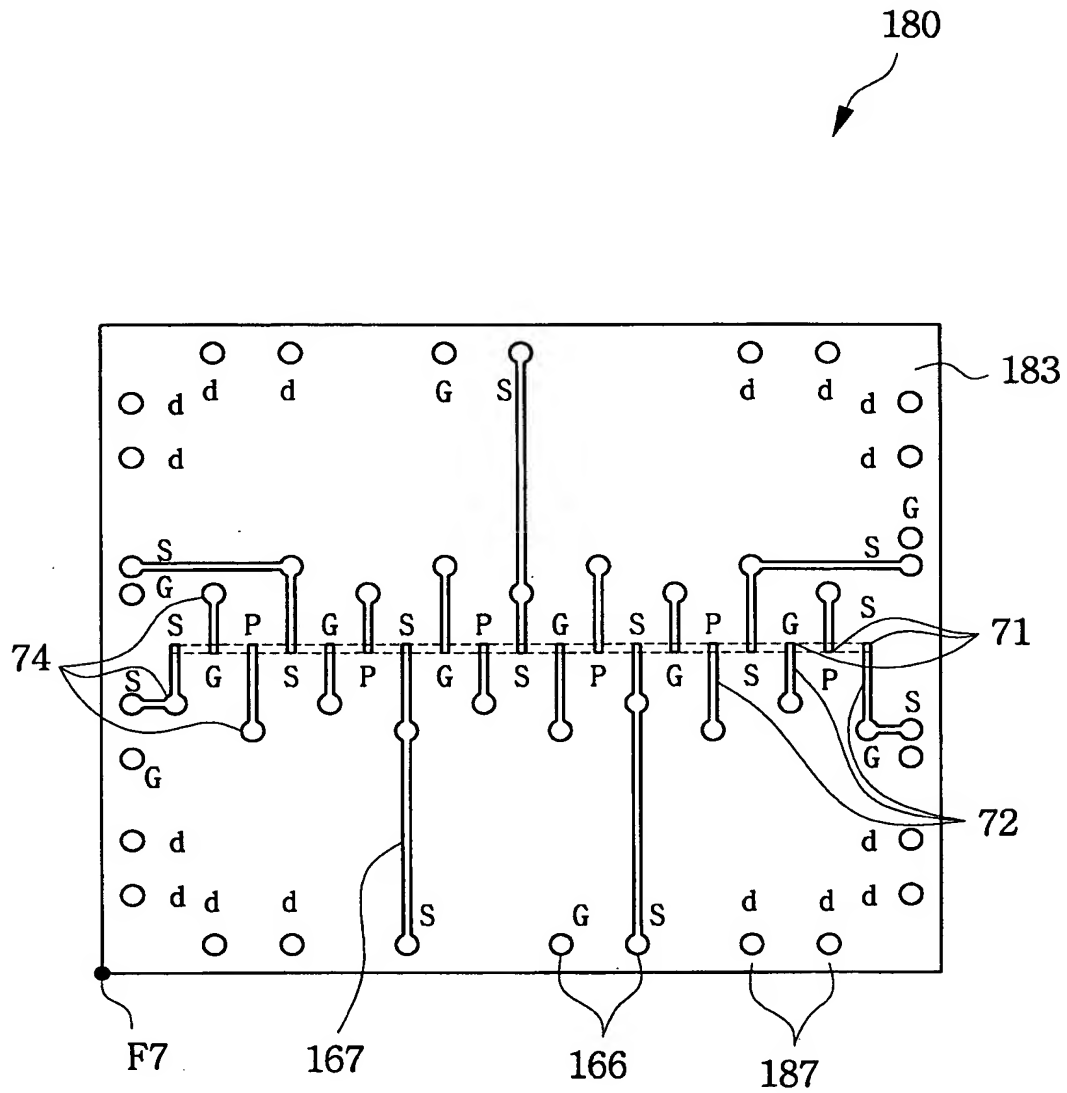


FIG. 13

